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# MICROSTRIP AMPLITUDE — WEIGHTED WILKINSON POWER DIVIDERS

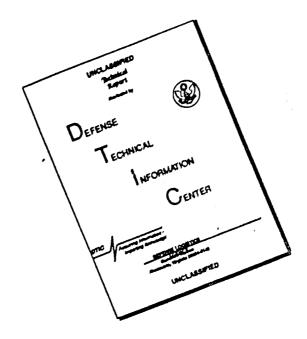
Keith D. Huck, 1LT, USAF

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# Microstrip Amplitude-Weighted Wilkinson Power Dividers

### 1. INTRODUCTION

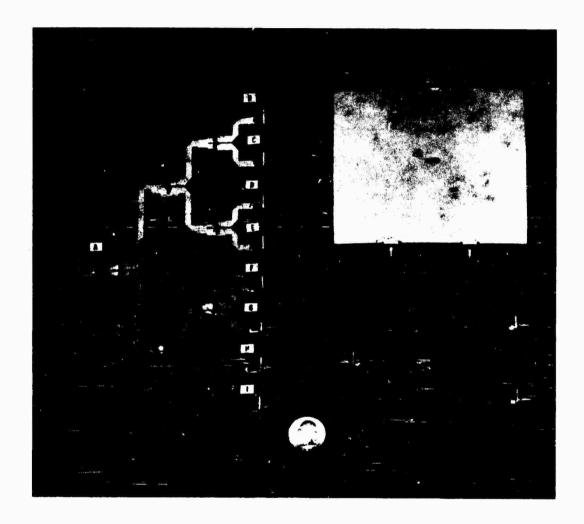
In array antennas, it is desirable to reduce sidelobe levels below the 13.2 (dB) that is typical of a uniformly illuminated array. The lower the sidelobe level, the less susceptible the antenna is to jamming. The easiest way to reduce sidelobe levels is with an amplitude taper, achieved by using attenuators or variable power dividers. The power divider method has the advantages of being less lossy, and less costly since a power divider will be required regardless of whether attenuators are used or not. The objective of this project was to develop a six-way microstrip power divider with -20 dB Chebyshev weighting.

### 2. GENERAL CONSIDERATIONS

To be used easily, the power divider should have equal phase at the outputs, allow for variable power division ratios, and have high output port isolation. Equal phase allows one to connect the power divider directly to the array elements without the need for trimmed line lengths. High output port isolation means that very little signal inserted into one output port is coupled into the other output port. The Wilkinson power divider was chosen because it has variable power division, equal

<sup>(</sup>Received for publication 6 March 1986)

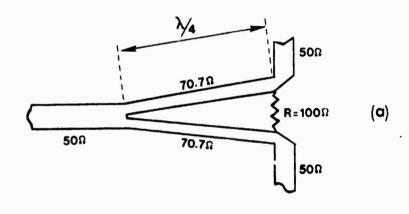
phase at the output ports, and high output port isolation. Single and multiple power divider circuits, a few of which are shown in Figure 1, were built on Rexolite 1422 double-sided copper clad substrates.



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### 3. WILKINSON POWER DIVIDER

The basic two section Wilkinson power divider consists of two equal impedance transmission lines connected to another transmission line of equal impedance by quarter wave transformers as shown in Figure 2a. A resistor is connected where the quarter-wave transformers meet the two output transmission lines. The resistor is called the isolation resistor and its purpose is to absorb energy coming in to one of the output ports and reflected from the power divider back into the other output port. The resistor also helps match all three ports. 1



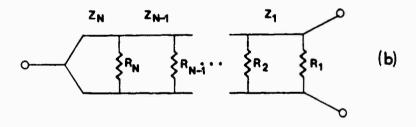


Figure 2. General Power Divider Design; (a) Two Stages and (b) Multiple Stages

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Howe, Jr., Harlan (1974) <u>Stripline Circuit Design</u>. Artech House, Dedham, Massachusetts

The circuit in Figure 2a is a  $50-\Omega$  line connected to two  $70.7-\Omega$  quarter-wave transformers in parallel, then to two 50 lines in parallel. The two  $70.7-\Omega$  lines in parallel are equivalent to one  $35.35-\Omega$  line

$$Z_{\text{teq}} = \frac{70.7 * 70.7}{70.7 + 70.7} = 35.35 \,\Omega \,. \tag{1}$$

The two 50- $\Omega$  lines in parallel are equivalent to one 25- $\Omega$  line

$$Z_{\text{out}_{eq}} = \frac{50.0 * 50.0}{50.0 + 50.0} = 25.0 \Omega$$
 (2)

Now we compare this example with the equation for quarter-wave impedance matching transformers.

$$Z_{t} = \sqrt{Z_{in}Z_{out}}$$

$$Z_{teq} = \sqrt{Z_{in}Z_{outeq}} = \sqrt{50 \cdot 25} = 35.36 \Omega.$$
(3)

Next, a third section is added. This section, a quarter-wavelength long, is called the compensation transformer and is used to match the two output arms with the input arm. The output VSWR is higher for the uncompensated power divider; but the input VSWR for the compensated power divider is better than that of the compensated power divider. The compensated power divider also has higher output port isolation.

Extra transformer stages can be added as needed in pairs (see Figure 2b). Each set of two transformers will increase the power divider bandwidth and reduce the output port VSWR. With each additional pair of transformers another resistor must be added. The more transformer pairs that are added, the more complex the circuit becomes and in addition, the line lengths become longer. Thus, the circuit has greater transmission line loss.

Cohn, S. B. (1968) A class of broadband three-port TEM-mode hybrids. IEEE Trans. Microwave Theory Tech., MTT-16(No. 2):110-116.

### 4. DESIGN AND LAYOUT OF A MICROSTRIP WILKINSON POWER DIVIDER

### 4.1 Design

The circuit is to be built on Rexolite 1422 (thickness h = 1/16 in., dielectric constant  $\epsilon_r = 2.56$ ) double sided 1-oz copper clad board, at frequency f = 7.5 GHz. The design formulas for the circuit shown in Figure 3 are: 1

$$K = \sqrt{P_b/P_a}$$
 (4a)

$$Z_1 = Z_{01} \left[ \frac{K}{1 + K^2} \right]^{1/4} \tag{4b}$$

$$Z_2 = Z_{01} \left[ K^{3/4} \left( 1 + K^2 \right)^{1/4} \right]$$
 (4c)

$$Z_3 = Z_{01} \left[ K^{-5/4} (1 + K^2)^{1/4} \right]$$
 (4d)

$$Z_4 = \sqrt{Z_{01}Z_{02}K}$$
 (4e)

$$Z_5 = \sqrt{Z_{01} Z_{02}/K} \tag{4f}$$

$$R = Z_{01} \left[ \frac{(1+K^2)}{K} \right] \tag{4g}$$

where

 $Z_1 - Z_5$  = the characteristic impedance of transformers T1-T5 respectively,

Z<sub>01</sub> \* the characteristic impedance of the input line,

 $z_{02}^{-s}$  the characteristic impedance of the left output line,

Z<sub>03</sub> \* the characteristic impedance of the right output line,

K = the voltage coupling ratio, and

R \* the value for the isolation resistor.

In all the circuits we have built,  $Z_{0.1} = Z_{0.2} = Z_{0.3} = 50 \Omega$ .

Since the circuit is microstrip, and the board has a low dielectric constant, the microstrip quarter wave transformers turn out to be more square than rectangular at the design frequency of 7.5 GHz. This was a difficult problem to overcome, since normally, two mitered bends are placed at the junctions of the first and second, and also the first and third transformers. However, square transformers

cannot be mitered without changing their electrical length. To maintain the equal phase at the outputs, the electrical line length of each path must be the same. To maintain the equal path lengths, the slot between T2 & T3 and T4 & T5 must be centered on the input line. The output ports must also be equi-distant from the center of the input. The transformer T1 can be offset to reduce the discontinuity effects. The isolation resistor bridges the slot, with its leads soldered to the junction between T2 & T4 and T3 & T5.

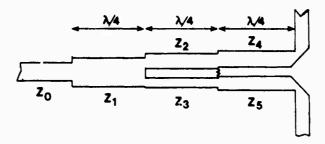


Figure 3. Compensated Five-Section Wilkinson Divider

### 4.2 Fabrication

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All circuits were drawn using a pen plotter consisting of a Calcomp 916 controller and a 1055 drum-type incremental plotter. The mask was made directly from the plot using standard photographic processes and then the circuit was etched, using standard photoresist techniques. Software to drive the plotter was written in FORTRAN5 and accessed an in-house developed graphics library also written in FORTRAN5.

The theory used to compute microstrip line width for a given impedance is described in References 3, 4 and 5. We have verified those formulas experimentally by constructing and testing uniform microstrip lines on various types of substrates.

<sup>3.</sup> Microwave Circuits: Theory and Application (1982) Continuing Education Institute.

Kirschning, M., and Jansen, R.H. (1982) Accurate model for effective dielectric constant of microstrip with validity up to millimeter-wave frequencies. <u>Electronics Lett.</u>, 18:272-290.

March, S. (1981) Microstrip packaging watch the last step. <u>Microwaves</u>, pp. 83-95.

The formulas used to compute the guide wavelength for the quarter-wave trans-

$$\lambda = \lambda_0 / \sqrt{\epsilon_{ef}}$$
 (5a)

$$\epsilon_{\text{ef}} = \epsilon_{\text{r}} - \frac{\epsilon_{\text{r}} - \epsilon_{\text{e}}}{1 + G(f/f_{\text{p}})^2}$$
 (5b)

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} F(W/h) - C$$
 (5c)

$$F(W/h) = (1 + 10 h/W)^{1/2}$$
 (5d)

$$C = \frac{\epsilon_r - 1}{4.5} \sqrt{\frac{t/h}{\tilde{W}/h}}$$
 (5e)

$$G = \sqrt{\frac{Z_0^{-5}}{60}} + 0.004 Z_0$$
 (5f)

$$f_{p} = Z_{o}/2\mu_{o}h \tag{5g}$$

where

 $\lambda =$ wavelength in microstrip.

 $\lambda_{\alpha}$  = free-space wavelength,

 $\epsilon_{ef}$  = frequency dependent  $\epsilon_{e}$ 

 $\epsilon_{\perp}$  = effective relative permittivity.

 $\epsilon_{\perp}$  : relative permittivity,

G = conductance.

f = design frequency.

W = strip width of microstrip line,

h = substrate thickness,

t - strip tinckness,

Z = characteristic impedance, and

 $\mu_{s}$  = free-space permeability.

Bahl, I.J., and Bhartia, P. (1981) Microstrip Antennas, Artech House, Dedham, Massachusetts.

### 5. TEST AND EVALUATION

### 5.1 Two-Way Power Divider

Eighteen single (two-way) power divider boards were built. The power ratios for the dividers extended from 1.0 to 5.0 in increments of 0.5 and were designed for both 4.0 GHz and 7.5 GHz center frequencies. The artwork for some of the devices are shown in Figures 4 to 8. First, the resistors were mounted on the top and the circuits tested from 2.0 to 12.0 GHz. After testing, the resistors were removed and remounted on the ground plane side of the board to reduce radiation loss from the resistors. This method, however, increased that radiation. The resistor leads were connected to the transmission lines on top through two holes drilled through the ground plane, dielectric, and transmission lines. The two two-way power dividers in Figure 1 show the different methods of mounting that resistor.

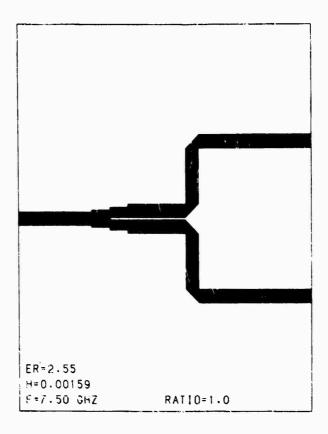


Figure 4. Artwork Pattern for a 1/1 Microstrip Divider, 7.5 GHz

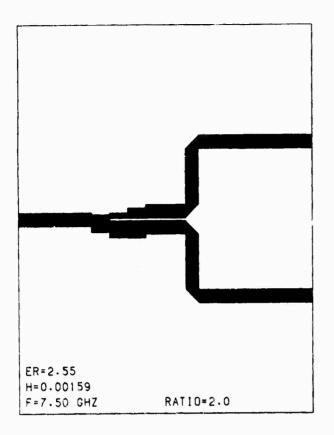


Figure 5. Artwork Pattern for a 2/1 Microstrip Divider, 7.5 GHz

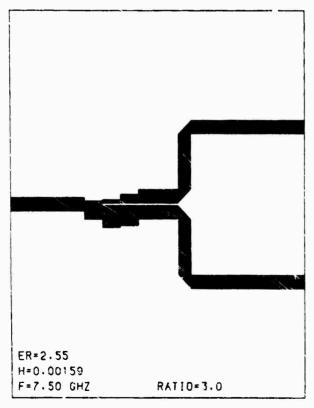


Figure 6. Artwork Pattern for a 3/1 Microstrip Divider, 7.5 GHz

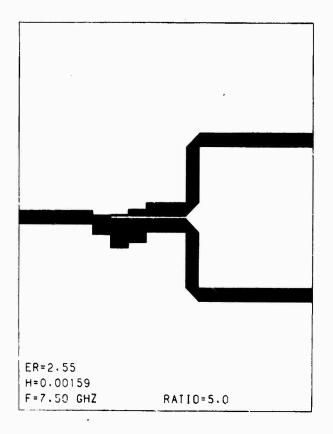


Figure 7. Artwork Pattern for a 5/1 Microstrip Divider, 7.5 GHz

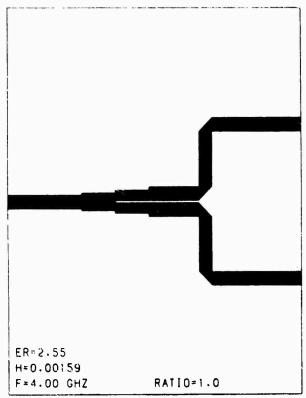


Figure 8. Artwork Pattern for a 1/1 Microstrip Divider, 4.0 GHz

Figures 9 to 13 are measured results for five of the circuits designed for 7.5 GHz center frequency. In these plots, the solid line represents the desired ratio of 10 log  $(P_a/P_b)$ . The curves labeled with (\*) are the measured ratio 10 log  $(P_a/P_b)$ , or simply the difference between the insertion loss measured at each arm. The symbols (+) and (x) are the measured insertion losses between each arm and the common input. The total power loss in the circuit, denoted by (), is not simply the sum of measured losses through each arm, but is defined as

$$IL_{total} = 20 \log_{10} \left\{ 10^{-(IL_L/20 + IL_R/20)} \right\}$$
 (6)

Although the greatest power loss is due to dielectric and conductor losses in the microstripline, there is some added loss at the higher frequencies due to reflections and radiation.

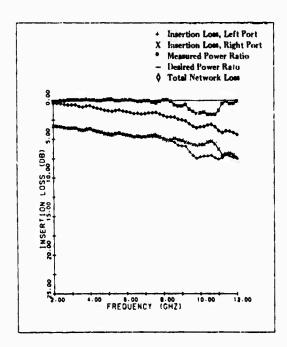
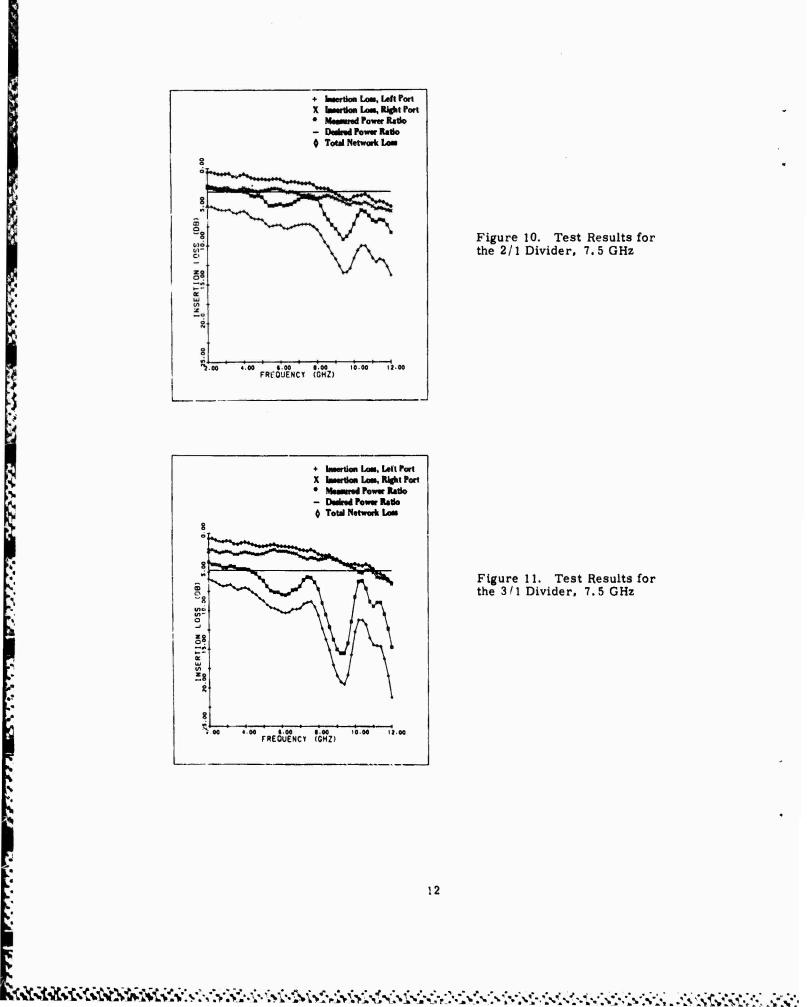
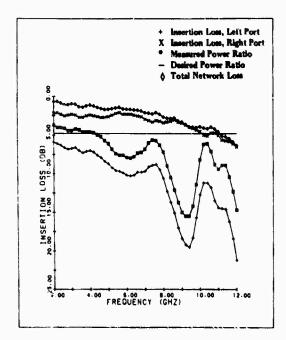


Figure 9. Test Results for the 1/1 Divider, 7.5 GHz





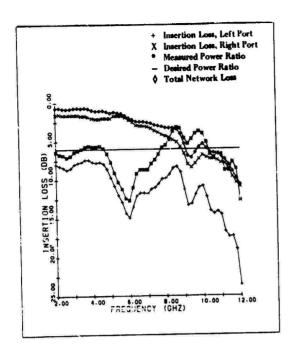


Figure 12. Test Results for the 4/1 Divider, 7.5 GHz

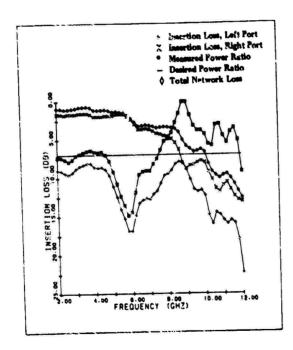


Figure 13. Test Results for the 5/1 Divider, 7.5 GHz

At very low frequencies (2 to 4 GHz) the measured power ratio is quite close to the design, but near the design frequency and above, its behavior is quite unpredictable, and grows worse with increasing power ratio. Figure 14 summarizes the results near the design frequency for this set of power dividers. The results are fairly good up to a 2.5/1 ratio. Beyond that, the actual ratio is much higher than desired. Surmising that the disparities were caused by radiation from the isolation resistor, we removed the resistor from the top surface of the board and remounted it on the bottom. The results, illustrated in Figures 15 and 16 were actually much worse. Evidently, the resistor leads projecting down through the transmission region are too much of a discontinuity, and reflect most of the power back to the input. We conclude that the best approach is to mount the isolation resistor on the top surface, with its leads soldered to the top of the microstriplines.

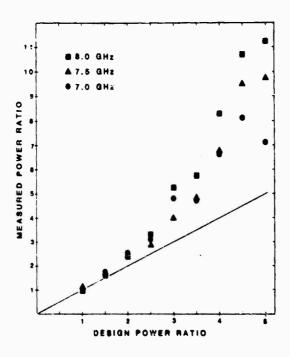


Figure 14. Comparison Between Design and Measured Power Ratio  $P_a/P_b$  for 7.5 GHz Circuits With Top-Mounted Resistor

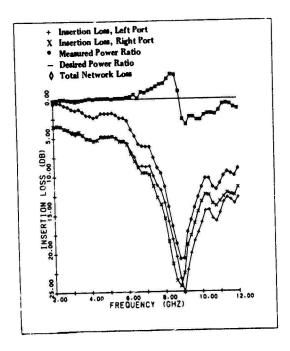


Figure 15. Test Results, 1/1 Divider, 7.5 GHz Bottom-Mounted Resistor

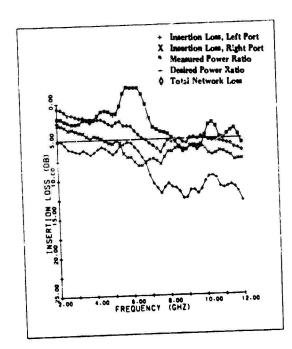


Figure 16. Test Results, 3/1 Divider, 7.5 GHz Bottom-Mounted Resistor

Figures 17 to 21 show measured results for five power dividers designed for 4 GHz. Over the 2 to 12 GHz frequency range, they performed better than the circuits designed for 7.5 GHz (see Figure 9). At and near the design frequency, the measured split ratios for these circuits were very close to the design  $P_a/P_b$  as shown in Figure 22. The fact that the 4 GHz dividers work so well is evidence that the design equations are valid. We cannot, however, predict the effects of the several discontinuities between transformer sections. As illustrated best by Figure 7, the artwork for the 5/1 divider, some of the sections are such low impedance that they are actually wider than they are long. In order to fit them in series with the other sections, we must offset them to the left or right. Especially at high frequencies, those junctions may introduce reflections, radiation, or multiple modes. Therefore, additional research will be required to design good power dividers for frequencies above 4 GHz.

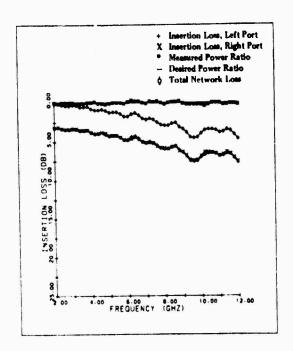


Figure 17. Test Results, 1.1 Divider, 4.5 GHz

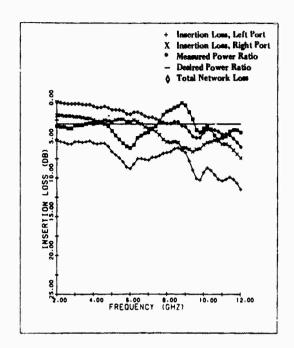
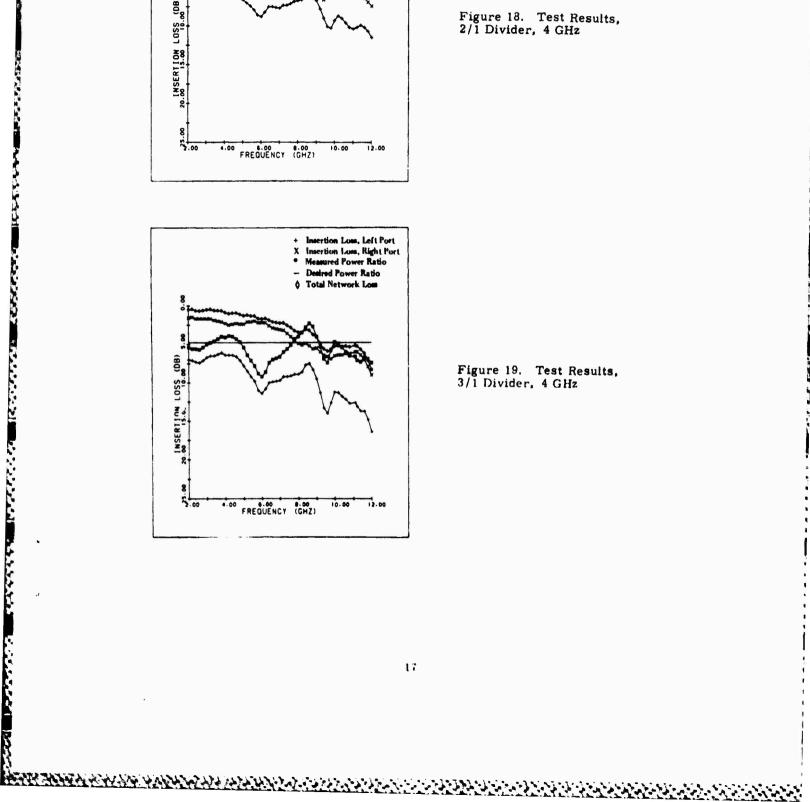


Figure 18. Test Results, 2/1 Divider, 4 GHz



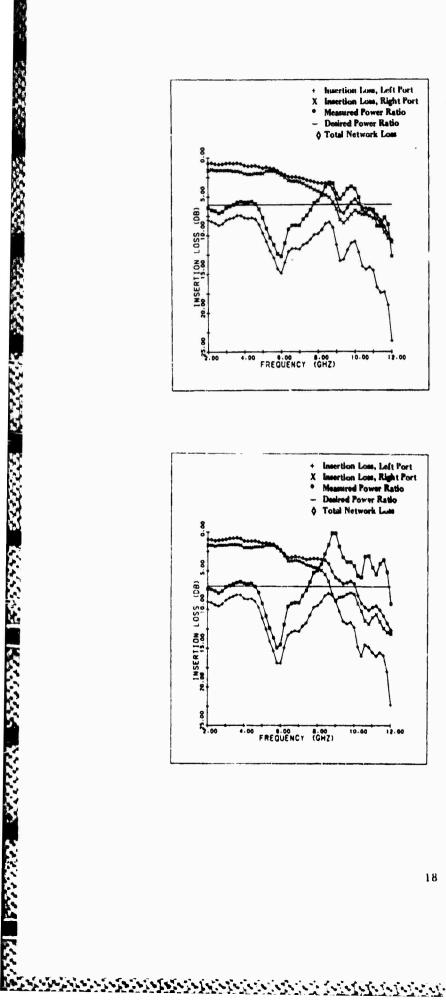


Figure 20. Test Results, 4/1 Divider, 4 GHz

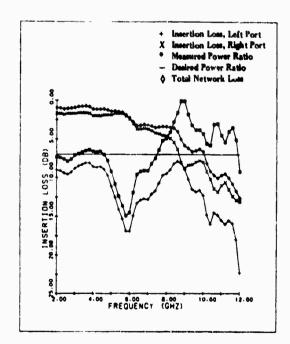


Figure 21. Test Results, 5/1 Divider, 4 GHz

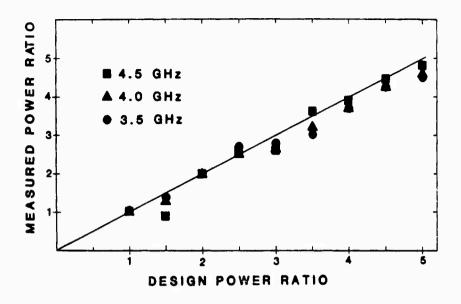


Figure 22. Comparison Between Design and Measured Power Ratio  $P_a/P_b$  for 4.0 GHz Circuits With Top-Mounted Resistor

### 5.2 Eight-Way Power Divider

Two multiple power divider boards were built for 7.5 GHz center frequency. The first was an eight-way divider with equal power to each port, shown in Figure 23. The second board was an eight-way power divider, with a 20 dB Chebyshev amplitude taper on the six inner ports, and equal power on each pair of outer ports (Figure 24).

These boards were tested using the automatic network analyzer to measure  $S_{12}$  from the common input to each of the eight outputs. The results are tabulated in Tables 1 and 2. At and below 6 GHz, the equal-split divider works very well, with both good amplitude balance and equal phase. The amplitude weighting on the unequal-split divider is closest to the design Chebyshev taper below 6 GHz. At the design frequency and above, the amplitude weights on the outer ports fall below the design values. This is consistent with the results of Figure 14—the split ratio is higher than desired, hence more power is directed to the center output ports.

At higher frequencies, for both of the eight-way circuits, the phase and amplitude errors are not symmetric. We have not been able to identify any particular cause, but the following are possibilities.

- (1) Discontinuities at the transformer junctions cause multiple reflections whose net effects are frequency-dependent.
- (2) Under or over-etching of the microstriplines will cause errors in the split ratios, because it alters their impedances.

- (3) The resistor and its leads disturb the fringing fields near the microstrip edges.
- (4) The close proximity of the two arms may alter the characteristic impedance as well as the guide wavelength.

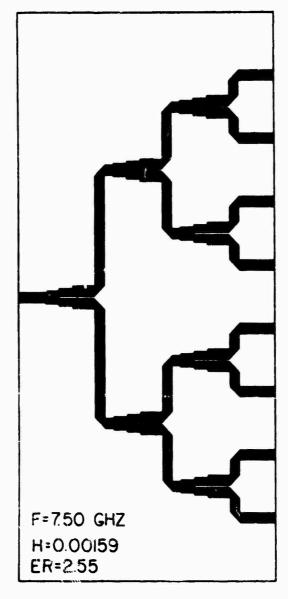


Figure 23. Artwork Pattern for Eight-Way Equal-Split Divider

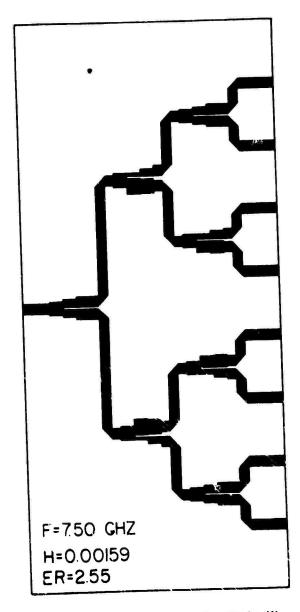


Figure 24. Artwork Pattern for Eight-Way Weighted Divider

Table 1. Measured Results, Eight-Way Equal-Split Divider

	Desired	Measured Pout		(dB)	Measure	(degrees)	
ARM No.	Pout (dB)	6.0 GHz	7.5 GHz	9.0 GHz	6.0 GHz	7.5 GHz	9. 0 GHz
1	0.0	-0.1	-0.2	-1.1	0	-2	-8
2	0.0	0.1	-0.3	-0.9	3	-4	-2
3	0.0	0. 1	-0.9	1.1	4	6	8 -2
4	0.0	-0.1	1.0	0.4	3	8	-2
5	0. 0	0. i	1.3	0.2	2	6	<del>-</del> 6
6	0, 0	0.1	-0.4	0.6	2	1_	7
7	0, 0	-0.1	-0.1	0.1	1	-8	-6
8	0.0	-0.1	0.7	-0.4	-4	-7	-8
Total	Power Loss	2.59	4.07	6.57			

Table 2. Measured Results, Eight-Way Weighted Divider

	Desired	Measured Pout		(dB)	Measure	(degrees)	
A RM No.	Pout (dB)	6. 0 GHz	7.5 GHz	9. 0 GHz	6.0 GHz	7.5 GHz	9. 0 GHz
1	-5, 34	-6.30	-6.60	-11.90	-4	-10	- 8
2	-5.34	-6.00	-7.80	-10.10	0	-10	-30
3	-2, 19	-1.80	-4.60	- 3.40	8	11	23
4	0.0	0.20	0.70	0.10	7	2	30
5	0, 0	0. <b>0</b> 0	0.00	0.00	4	- 2	7
6	-2, 19	-2.80	-4.70	- 3,80	5	3	8
7	-5.34	-5.90	-7.90	-11.30	-4	- 8	7
8	-5, 34	-6.10	-7.20	-11.90	- 8	-10	- 8
Total	Power Loss	3. 14	3, 94	7.57			

### 6. CONCLUSIONS AND RECOMMENDATIONS

In attempting to construct unequal-split microstrip power dividers for amplitude weighting of array antennas, we have noted some difficulties in both design and fabrication. Many of those resulted from the choice of substrate ( $\epsilon_r = 2.54$ , h = 1/16 in.) which requires drastic variations in line widths for the characteristic impedances we needed. The resulting circuit layouts have a number of step dis-continuities, whose net effect is difficult to predict. However, the very good results in amplitude and phase accuracy achieved with the 4 GHz dividers shows that split ratios of 7 dB or greater can be achieved with the Wilkinson design.

Some possible improvements to our power divider design are:

- (1) Taper the junctions between transformer sections wherever possible. Tapering should extend the bandwidth and reduce random errors by eliminating discontinuities.
- (2) Use low-profile chip-type resistors, to reduce radiation and reflection caused by the resistor leads.
- (3) Use a  $100\,\Omega$  impedance for the input and output lines (instead of  $50\,\Omega$ ). This would cause all the transformer impedances to double resulting in thinner microstriplines throughout.

The above changes should improve the performance of dividers with small split ratios (~ 5 dB or less). For larger ratios, branch-line and rat-race couplers should be examined.

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